PATENT
ATTY. DOCKET NO. IBM/145DV1
Confirmation No. 3332

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Mark Kenneth Hoffmeyer et al.	Art Unit:	2827
Serial No.	: 09/924,711	Examiner:	Jose H. Alcala
Filed	: August 8, 2001		
For	: PROCESSING OF CIRCUIT BOARDS WITH PROTECTIVE, ADHESIVE-LESS COVERS ON AREA ARRAY BONDING SITES		

Cincinnati, Ohio 45202

May 1, 2003

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37CFR 191)

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal received by the Office on March 6, 2003.

2. **STATUS OF APPLICANT**

This application is on behalf of

XX **other than a small entity**

____ small entity

Verified Statement:

___ attached

___ already filed

3. **FEE FOR FILING APPEAL BRIEF**

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

____	Small entity	$160.00
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4. **EXTENSION OF TIME**

Applicant petitions for an extension of time under 37 C.F.R. 1.136(a) for the total number of months checked below:

Months		Fee for other than small entity	Fee for small entity
_____	one month	S 110.00	S 55.00
_____	two months	..... 400.00	..... 200.00
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_____	four months	..... 1,440.00	..... 720.00
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If an additional extension of time is required, please consider this a petition therefor.

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The total fee due is:

Appeal Brief Fee **$320.00**

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6. **FEE PAYMENT**

XX Attached is a check in the sum of **$320.00**.

____ Charge fee to Deposit Account No. 23-3000.

7. **FEE DEFICIENCY**

XX Charge any additional extension fee required or credit any overpayment to Deposit Account No. 23-3000.

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CERTIFICATE OF MAILING 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 1, 2003.

_____
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte Mark Kenneth Hoffmeyer, Daniel Scott Johnson

Appeal No. _____
Application No. 09/924,711

APPEAL BRIEF

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Applicant:	Mark Kenneth Hoffmeyer et al.	Art Unit:	2827
Serial No.:	09/924,711	Examiner:	Jose H. Alcala
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APPEAL BRIEF

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I. REAL PARTY IN INTEREST

This application is assigned to International Business Machines Corporation, of Armonk, New York.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

This application is a divisional of U.S. Patent Application Serial No. 09/606,583 (now issued as U.S. Patent No. 6,499,215), and was originally filed with 22 claims. During prosecution, claims 1-10 and 13-18 were canceled, claims 11 and 19 were amended, and claims 23-32 were added. Claims 11-12 and 19-32 are therefore currently pending. All such claims currently stand rejected, and are now on appeal.

IV. STATUS OF AMENDMENTS

There have been no amendments filed subsequent to final rejection (Paper No. 8).

V. SUMMARY OF INVENTION

The invention is generally related to the processing of circuit boards containing area array surface treated bonding sites, such as noble metal terminal pads of a Land Grid Array (LGA) assembly.

As noted, for example, at pages 1-4 of the Application, area arrays such as LGA's, Ball Grid Arrays (BGA's), Column Grid Arrays (CGA's) and the like often complicate the fabrication processes used to process circuit boards upon which such area array bonding sites are disposed. In particular, area arrays may have surface finish treatments that need to be kept free of contaminants to ensure reliable electrical interconnection with attached area array components. However, some fabrication processes that are applied to other areas of a circuit board, such as soldering, masking, screen printing, cleaning, and reworking, can potentially introduce contaminants such as flux residues, solder, and various adherent or semi-adherent organic and inorganic residues to the area array bonding sites, and hence it is desirable to protect these sites from contamination during these processes.

Contamination of an area array bonding site may result in the short circuiting of adjacent conductors and/or poor conduction for individual conductors. Furthermore, such problems may not even manifest until some time after processing of the circuit board is complete, and the circuit board has been installed in a product. As a result, significant reliability concerns are raised by contamination of area array bonding sites.

Conventionally, area array bonding sites have been protected during various processing steps through the temporary application of an adhesive film. However, it has been found that protection of the bonding sites with tape masking may introduce a separate source of contamination when a portion of the tape, or the adhesive residue from the tape, remains on the bonding site. Such residue may entrap fluids during further processing of the circuit board, and may otherwise encourage condensation and retention of water. In addition, the tape residue itself, or contaminants entrapped during processing of the circuit board, may detrimentally chemically react with the circuit board.

To address these concerns, Applicants have developed a removable, protective cover for use in overlaying and protecting an array area bonding site on a circuit board during fabrication processing. For example, as shown in Fig. 1 of the Application (which is reproduced below for

the convenience of the board), a protective cover 10 may overlay a portion of a circuit board 12 having an area array surface treated bonding site 14:

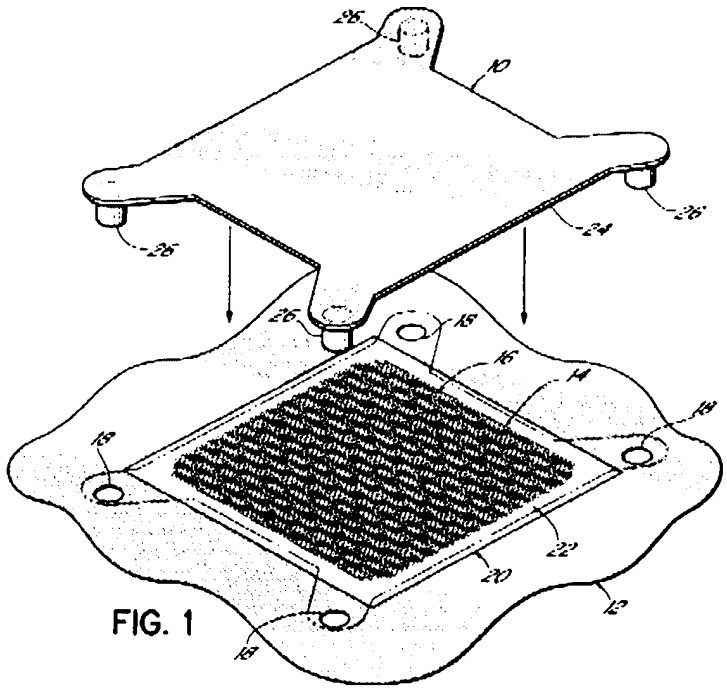


FIG. 1

Patterned about the bonding site 14 are a plurality of apertures 18 forming a footprint 20 that encompasses the bonding site 14 with a margin 22. Desirably, the margin is selected to be suitably broad to prevent contaminants from reaching the outermost pad terminations 16 while not unduly reducing the portion of the circuit board 12 available for processing. (Application, page 8). The protective cover 10 is formed from a base material 24 shaped to correspond to the footprint 20, and desirably resistant to the processing of the circuit board 12, e.g., FR4 glass epoxy laminate. (Application, page 8). Given the use in protecting the underlying area array bonding site, the base material is therefore non-conductive throughout the region that overlays the bonding site.

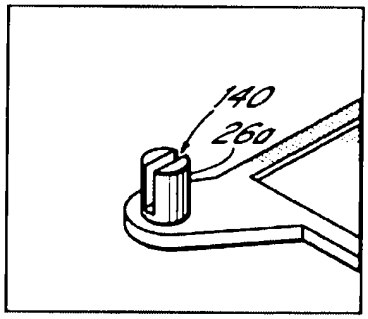
To register the cover with the circuit board, a plurality of posts 26 are registered on the base material 24 to correspond to the pattern of apertures 18 on the circuit board 12. (Application, page 9). As a result, in use the cover is placed on the circuit board with the posts 26 inserted into the apertures 18 such that the bonding site is overlaid by the cover. It should be

noted, however, that in some embodiments, the posts may be attached to the circuit board, with the apertures disposed in the protective cover. (Application, page 9).

Thus, whenever it is desired to protect a bonding site during processing of a circuit board, the protective cover 10 may simply be placed over the bonding site, with the posts used to properly align the cover, and typically assist in removably retaining the cover in place on the circuit board. Processing may then proceed, with the cover protecting the bonding site. Once processing is completed, the cover may then be removed, thereby enabling further processing, such as securing a component to the area array bonding site, to be completed.

Additional aspects of the invention, which are set forth in some of the pending claims, include, for example, the use of a base material that is about 0.006-0.008" thick. As discussed at page 9 of the Application, such a base material may be particularly advantageous when a custom stencil is used in certain screen printing operations, as a protective cover may remain in place on the circuit board while screen printing is performed.

In addition, in some embodiments, it may be desirable to use diametral slots in the posts to assist in retaining each post in its corresponding aperture. For example, as shown in Fig. 10 (the relevant portion of which is reproduced below for the convenience of the Board), diametral slots 140 may be formed in posts 26a, as follows:



The diametral slots serve to permit the resulting fingers in the ends of the posts to deflect inwardly when the posts are inserted into the apertures, and thereafter apply an outwardly directed force to the walls of the apertures to reduce the possibility of a cover becoming dislodged during movement, tipping or handling of the circuit board during various fabrication processes.

As such, the protective cover recited in the pending claims serves to protect delicate area array bonding sites during circuit board fabrication processes in a substantially less intrusive manner, and with a reduced risk of introducing additional sources of contamination, as compared to the adhesive tapes that have conventionally used for essentially the same purpose.

VI. ISSUES

A. Whether claims 11-12, 19-21, 23-26, and 29-31 were improperly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,750,092 to *Werther*.

B. Whether claims 22 and 27 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,750,092 to *Werther* in view of U.S. Patent No. 5,413,489 to *Switky*.

C. Whether claims 28 and 32 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,750,092 to *Werther*.

VII. GROUPING OF CLAIMS

Claims 11-12 and 19-32 do not stand or fall together.

VIII. ARGUMENT

Applicants respectfully submit that the Examiner's rejections of claims 11-12 and 19-32 are not supported on the record, and that the rejections should be reversed. Reversal of all rejections, and passage of this case onto allowance, are therefore respectfully requested.

A. Claims 11-12, 19-21, 23-26, and 29-31 were improperly rejected under 35 U.S.C. § 102(b) as being anticipated by *Werther*.

The Examiner argues that *Werther* anticipates all of claims 11-12, 19-21, 23-26, and 29-31. Anticipation of a claim under 35 U.S.C. §102, however, requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros., Inc. v. Union Oil Co., 2 USPQ2d 1051, 1053 (Fed. Cir.

1987), *quoted in* In re Robertson, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999). Absent express description, anticipation under inherency requires extrinsic evidence that makes it clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991), *quoted in* In re Robertson at 1951. "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Continental Can at 1749, *quoted in* In re Robertson at 1951.

Applicants respectfully submit that *Werther* does not disclose the various features recited in claims 11-12, 19-21, 23-26, and 29-31, and as such, the rejections thereof should be reversed. Applicants will hereinafter address the various claims that are the subject of the Examiner's rejection in order.

Claim 11

Turning first to independent claim 11, this claim recites an assembly comprising a circuit board, an area array bonding site on a surface of the circuit board, and a protective cover overlaying the bonding site. The protective cover is removably registered to the bonding site by a plurality of posts secured to one of the protective cover and the circuit board into a plurality of apertures disposed in the other of the protective cover and the circuit board. Moreover, claim 11 recites that the protective cover is non-conductive throughout at least a region thereof that overlays the bonding site.

Applicants respectfully submit that *Werther* does not disclose this combination of features, and as such, the Examiner has failed to meet the burden required to sustain a rejection under 35 U.S.C. §102(b).

As described in the Application, the structure of claim 11 is used to protect sensitive area array bonding sites from contamination during manufacture, and prior to mounting of active surface mounted components such as integrated circuit (IC) packages. Consistent with the contamination-prevention nature of the claimed protective cover, the cover is recited to be non-conductive throughout the region of the bonding site that is being protected by the cover.

Werther, on the other hand, discloses a package structure that is utilized to interconnect a semiconductor chip to a circuit board. *See, e.g.*, Fig. 1 of *Werther*, which is reproduced below for the Board's convenience:

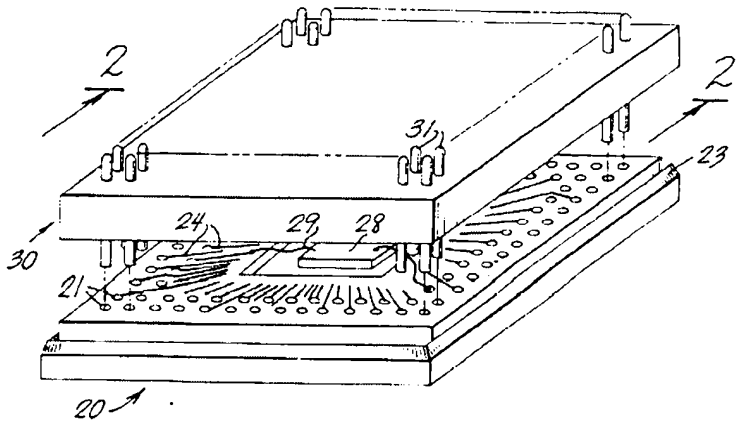


Fig. 1 of *Werther*, in particular, discloses an injection molded pin grid array 30 having a "picture frame" array of conductive pins 31 that is used to electrically interconnect the semiconductor chip to a circuit board. The manner in which this is accomplished is via a conductive pattern 24 and an array of conductive pin recesses 21 formed in a base 20. A semiconductor chip is mounted to base 20, and the conductive pattern 24 includes traces that extend from specific I/O pads on the semiconductor chip to specific pin recesses 21. As a result, when pin grid array 30 is aligned over base 20, the conductive pins 31 in the array are received in the pin recesses 21, thus completing the electrical interconnection with the semiconductor chip. The pin grid array 30 and base 20 are thereafter ultrasonically welded to one another to complete the package. After welding, the opposite ends of the conductive pins 31 remain exposed for the purpose of electrically and mechanically connecting the package to a circuit board.

The Examiner apparently analogizes pin grid array 30 to a protective cover within the context of claim 11. However, while pin grid array 30 is formed of a molded, and presumably non-conductive material, the specific nature of this body in conducting electrical signals between a semiconductor chip and a circuit board in use precludes its utilization as a "protective cover" as is required by claim 11.

In particular, the Board will note that the structure on top of base 20, which the Examiner analogizes to a bonding site, comprises the conductive pattern 24, as well as the array of conductive pin recesses 21. This region extends nearly across the entire top surface of base 20. More importantly, however, the pin grid array 30 is not non-conductive throughout this entire region, given that the conductive pins 31 by necessity must overlap and align with their corresponding pin recesses 21 (which fall within the area of the bonding site).

As such, *Werther* cannot be read to disclose a "protective cover being non-conductive throughout at least a region thereof that overlays [a] bonding site", as is recited in claim 11.

The Examiner apparently attempts to take the position that the protective cover 30 of *Werther* is non-conductive, arguing that "while the pins 31 are conductive, the protective cover of the Werther reference is not conductive 'per se'" (Advisory Action, page 2). It appears as if the Examiner is attempting to separate the pins 31 from the non-conductive material in array 30, and argue that the everything in the pin grid array, except for the pins, is non-conductive.

Such an interpretation on the part of the Examiner, however, runs counter to the language of claim 11. In particular, the claim recites that the protective cover is non-conductive throughout the region of the bonding site that is being protected by the cover. Applicants submit that the inclusion of conductive pins, or any other conductive material, in a structure that is claimed to be "non-conductive" throughout a particular region, effectively renders that structure "conductive" at least in those areas where the conductive material is present. Thus, the presence of any conductive material in a structure that falls within the region of a bonding site being overlayed by such a structure, results in that structure falling outside of the scope of claim 11.

Claim 11 is therefore novel over *Werther*, and the rejection thereof should therefore be reversed.

Applicants also respectfully submit that claim 11 is non-obvious over *Werther*, as there is no suggestion in the reference, or elsewhere in the prior art, to modify the pin grid array of *Werther* to be non-conductive throughout a region that overlaps a bonding site. Indeed, modifying the *Werther* assembly in this manner would render the modified assembly unsatisfactory for its intended purpose, which has been found to be persuasive evidence of non-

obviousness.[1]. Were no conductive material provided in the region of pin grid array 30 that overlaps the bonding site on base 20, the semiconductor chip would effectively be incapable of receiving or transmitting electrical signals externally from the package within which it is housed, or receiving any form of power. The chip would therefore be completely useless.

Furthermore, it is important to note that *Werther* is directed to an entirely different problem than that of protecting a bonding site from contamination during manufacture. Indeed, the purpose of *Werther* is to facilitate conductivity through the pin grid array, rather than inhibit conductivity, as is desirable for a protective cover such as that recited in claim 11. As such, Applicants respectfully submit that one of ordinary skill in the art would not look to *Werther* to provide a structure for a protective cover to provide contamination protection for a bonding site in the manner recited in claim 11.

Applicants therefore respectfully submit that claim 11 is also non-obvious over the prior art of record. Reversal of the Examiner's rejection of this claim, and a favorable determination of patentability for the claim, are therefore respectfully requested.

Claim 12

Claim 12 is not argued separately.

Claim 19

Next, with respect to independent claim 19, this claim recites a cover for protecting an area array bonding site on a surface of a circuit board, where the circuit board has a plurality of apertures. The cover includes a base member having a first face and a second face, and shaped to at least correspond to the area array bonding site. The cover additionally includes a plurality of posts coupled to the first face and registered for the plurality of apertures. Moreover, as with claim 11, claim 19 recites that the base member is non-conductive throughout at least a region thereof that is configured to overlay the bonding site. Thus, this claim also highlights the

[1]"If [a] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." MPEP §2143.01 (*citing* In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

principal nature of the cover as a temporary, protective device used during manufacture of a circuit board to protect a bonding site from contamination.

As noted above in connection with claim 11, *Werther* does not disclose or suggest a configuration whereby a protective cover, and in particular, a base member thereof, is non-conductive throughout a region that overlays a bonding site. The simple presence of conductive pins in the *Werther* structure renders the structure conductive in at least a portion of the region being overlaid by the structure. The rejection of claim 19 should therefore be reversed for the same reasons presented above for claim 11. Reversal of the Examiner's rejection, and a favorable determination of patentability for the claim, are therefore respectfully requested.

Claims 20-21, 23-26, and 29-31

Claims 20-21, 23-26, and 29-31 are not argued separately

B. Claims 22 and 27 were improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Werther* in view of *Switky*.

Applicants respectfully submit that the Examiner's obviousness rejections of claims 22 and 27 based upon U.S. Patent No. 4,750,092 to *Werther* in view of U.S. Patent No. 5,413,489 to *Switky* are not supported on the record, and that the rejections should be reversed.

A *prima facie* showing of obviousness requires that the Examiner establish that the differences between a claimed invention and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. §103(a). Such a showing requires that all claimed features be disclosed or suggested by the prior art. Such a showing also requires objective evidence of the suggestion, teaching or motivation to combine or modify prior art references, as "[c]ombining prior art references without evidence of such a suggestion, teaching or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability -- the essence of hindsight." In re Dembiczak, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

Applicants respectfully submit that, in the instant case, the Examiner has failed to establish a *prima facie* case of obviousness as to claims 22 and 27, and as such, the rejections should be reversed.

Each of claims 22 and 27 recites the use of "diametral slots" in the claimed posts. As discussed above, the diametral slots (one implementation of which is shown in Fig. 10 of the Application), facilitate the engagement of the posts with their corresponding apertures due to the ability for the resulting "fingers" formed in the posts to deform inwardly when inserted into the apertures and thereby apply an outwardly-directed force to the walls of the apertures. As a result, the posts are less likely to disengage when the circuit board is manipulated during processing.

In rejecting these claims, the Examiner admits that *Werther* fails to teach posts with diametral slots. (November 6, 2002 Office Action, page 5). However, the Examiner instead relies on *Switky*, and in particular screws 46 thereof (*see, e.g.*, Fig. 1) for allegedly disclosing posts with diametral slots.

Applicants respectfully submit, however, that *Switky* does not disclose posts with diametral slots, as alleged by the Examiner, and as such, the proposed combination does not render claims 22 and 27 obvious. There is simply no disclosure in *Switky* that any of screws 46 include diametral slots as recited in the claims. Certainly, none of the figures in *Switky* illustrate any feature that is analogous to a diametral slot on any of screws 46, and there is no passage in the specification that describes any such feature. As a result, no motivation has been established for modifying *Werther* to include slotted posts, as proposed by the Examiner. Therefore, claims 22 and 27 are non-obvious over the combination of *Werther* and *Switky*, and the rejections thereof should be reversed.

Reversal of the Examiner's rejections of these claims, and a favorable determination of patentability therefor, are therefore respectfully requested.

C. Claims 28 and 32 were improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Werther*.

Next, with respect to claims 28 and 32, these claims recite that the protective cover (claim 28) or the base member (claim 32) have a thickness of about 0.006 to about 0.008 inches.

In rejecting these claims, the Examiner simply discounts the additional features as being nothing more than design choices, based upon a supposed well known motivation "to reduce the thickness of elements or layers in order to improve integration in semiconductor devices or packages." (November 6, 2002 Office Action, page 5).

However, this motivation relied upon by the Examiner is entirely irrelevant to the claims at issue. The claims focus on a removable protective cover used during fabrication processes, and not on a semiconductor package or device. Indeed, as noted above in Section V, a principal motivation for utilizing the claimed thickness is to enable the cover to remain in place during screen printing operations. The reduced thickness enables a custom stencil to be overlaid on a circuit board with the cover still in place, and thus enable screen printing to proceed without having to remove the cover.

While different rationales may be applied to motivate one of ordinary skill in the art to modify the teachings of a reference, in this instance, the fact that *Werther* is not even directed to a protective cover for an area array bonding site renders the Examiner's proposed motivation irrelevant to the claims at issue. Applicants therefore respectfully submit that the Examiner has failed to establish a sufficient motivation to modify *Werther* to utilize a material having a thickness within the recited range. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness as to claims 28 and 32, and the rejections thereof should be reversed.

Reversal of the Examiner's rejections of these claims, and a favorable determination of patentability therefor, are therefore respectfully requested.

IX. CONCLUSION

In conclusion, Applicants respectfully request that the Board reverse the Examiner's rejections of claims 11-12, and 19-32, and that the Application be passed to issue. If there are any questions regarding the foregoing, please contact the undersigned at 513/241-2324. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

WOOD, HERRON & EVANS, L.L.P.

Date: 1 MAY 2003

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